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1	5883814.pn. and layout\$4 same (mod\$4 chang\$4 custom\$4)
2	5883814.pn. and processor same logic
3	5883814.pn. and layout\$4 same (mod\$4 custom\$4 chang\$4 custom\$4)
4	"20040088667" and closed
5	"20040088667" and closed same signal same transfer\$4
6	"20040088667" and closed same signal same transfer\$4 same (var\$5 known)
7	"20040088667" and closed same signal same transfer\$4 same (known)
8	"20040088667" and closed same signal same transfer\$4
9	5883814.pn. and layout\$4 same (mod\$4 chang\$4 custom\$4) and DRAM
10	5883814.pn. and DRAM same (chang\$4 mod\$7)
11	5883814.pn. and DRAM same (chang\$4 modif\$7)
12	5883814.pn. and signal adj transfer\$4
13	"20040088667" and signal adj transfer\$4
14	"20040088667" variable same chang\$4 same layout same component
15	"20040088667" and variable same chang\$4 same layout same component
16	5883814.pn. and layout\$4 same (mod\$4 chang\$4 custom\$4)
17	5883814.pn. and (mod\$4 chang\$4 var\$8)
18	"20040088667" and fixed
19	5883814.pn. and cpu
20	5883814.pn. and processor
21	5883814.pn. and processor near4 logic and peripheral
22	5883814.pn. and controller
23	5883814.pn. and (controller processor logic)
24	5883814.pn. and (controller processor logic) same (circuit component) same (signal transfer\$4)
25	5883814.pn. and (logic same component) interface peripheral resgister
26	5883814.pn. and ((logic near3 (component circuit macro)) interface peripheral resgister)
27	5883814.pn. and ((logic near3 (component circuit macro control)) interface peripheral resgister)
28	5883814.pn. and (peripheral resgister)
29	5883814.pn. and (timing) same (anal\$4 verif\$4 eval\$4 test\$4)
30	5883814.pn. and (timing) same (anal\$4 verif\$4 eval\$4 test\$4 sim\$7 emul\$7)
31	5883814.pn. and (clos\$4 integrated)
32	5883814.pn. and (clos\$4 integrated embed\$4 soc system near3 chip)
33	"20040088667" and new same add\$4 same circuit same variable
34	"20040088667" and new same add\$4 same circuit same variable
35	"20040088667" and dram with (grow\$4 add\$4 expan\$6 ecten\$5)
36	"20040088667" and dram with (grow\$4 add\$4 expan\$6 exten\$5)
37	5883814.pn. and dram with (grow\$4 add\$4 expan\$6 exten\$5)
38	"20040088667" and new\$4 same add\$4 same circuit same variable
39	5883814.pn. and (auxiliary peripheral)
40	5883814.pn. and DRAM same (chang\$4 mod\$7 custom\$7 var\$8)
41	5883814.pn. and DRAM same (chang\$4 modif\$7 custom\$7 var\$8)
42	5883814.pn. and DRAM same (chang\$4 modif\$7 custom\$7 var\$8 subdivi\$7 restuct\$7)
43	"20040088667" and straight near3 path
44	5883814.pn. and straight
45	"20040088667" and available with fill\$4
46	"20040088667" and (available exten\$5 expan\$5 fill\$4)

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47	5883814.pn. and add\$7
48	5883814.pn. and (add added addition)
49	"20040088667" and (available exten\$5 expan\$5 amount fill\$4)
50	5883814.pn. and (empty grow\$4 exten\$4 expan\$6 reser\$4 available)
51	5883814.pn. and (empty grow\$4 differ\$5 amount memory exten\$4 expan\$6 reser\$4 available)
52	5883814.pn. and (noise coupl\$5 decoupl\$4 capacit\$5 bypass by adj pass\$4)
53	5883814.pn. and (noise coupl\$5 decoupl\$4 capacit\$5 bypass by adj pass\$4) same fig
54	5883814.pn. and (noise coupl\$5 decoupl\$4 capacit\$5 bypass by adj pass\$4) same fig.
55	5883814.pn. and (noise coupl\$5 decoupl\$4 capacitance capacitor bypass by adj pass\$4)
56	5883814.pn. and layout same (modif\$4 flex\$4 var\$6 chang\$4 adjust\$4 meet grow\$4 exten\$5 expan\$4)